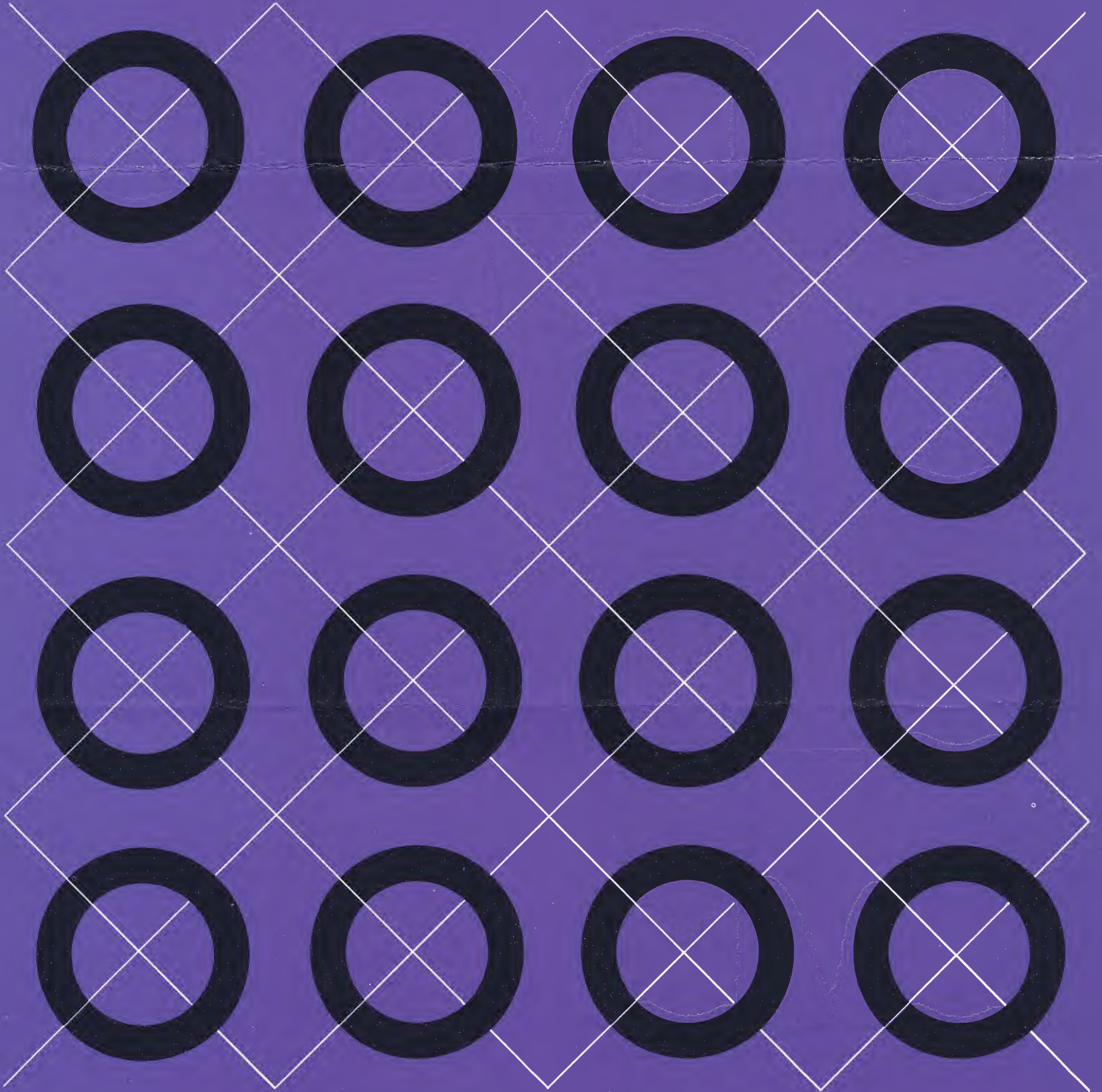
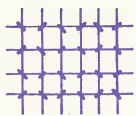


ministore III

a new low cost core memory



ministore III



A complete, low cost, random access storage system with wide application in the following areas:
Input/Output buffering ■ Tape storage ■ Data communications ■ Format control ■ Special purpose data systems ■ Small computer working memory

a value engineered magnetic core

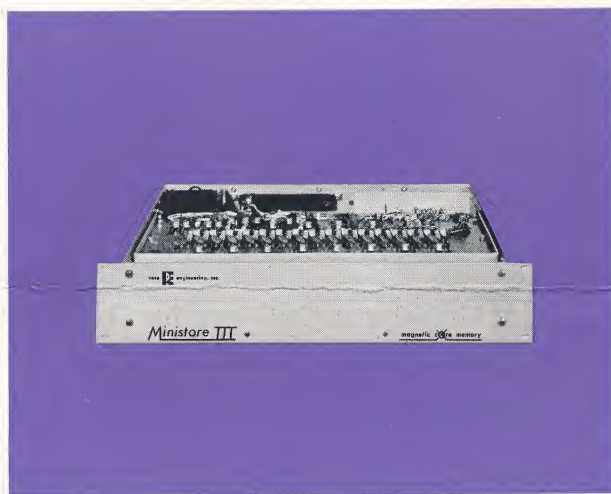
DESCRIPTION. The MINISTORE III is a general purpose random access magnetic core memory containing a magnetic core array, input/output data register, sense amplifiers, digit drivers, current drivers, address storing current switches, and power regulators. The data access time of the MINISTORE III is less than 4 μ sec. A complete Read/Regenerate cycle or a Clear/Write cycle takes 10 μ sec.

The MINISTORE III is available in various sizes containing up to 1024 discrete address locations in which up to 8 bits of data may be stored. The address locations are

expressed in pure binary format. Data is stored and retrieved in parallel form. All inputs and outputs operate at standard transistor logic levels, 0 and -6 volts.

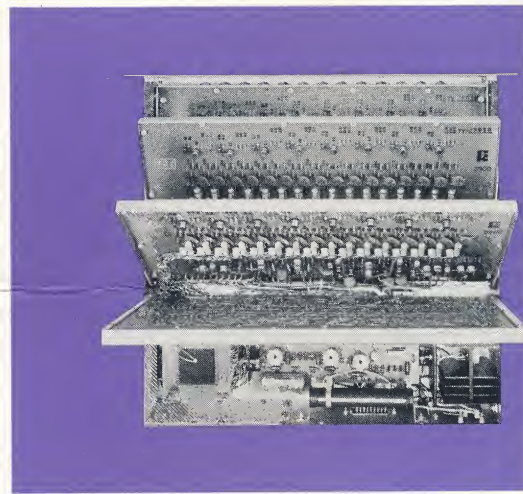
OPERATION. Addressing of the memory is straight binary, two lines per bit, providing a unique location for all addresses from the first to the maximum address. The memory operates on either a Read/Regenerate (Unload) or a Clear/Write (Load) cycle. The memory operates in the same manner in both the UNLOAD cycle and the LOAD cycle, the only difference being the application of a LOAD or UNLOAD level to signal the memory

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DESIGNED FOR VALUE

MINISTORE III represents a significant step forward in the application of VALUE ENGINEERING techniques. It incorporates a novel design which utilizes the charging and discharging current of capacitors to switch the magnetic state of memory cores. This circuit requires fewer active components. Hence the major attraction of the MINISTORE III is its very low price which ranges from $\frac{1}{3}$ to $\frac{1}{2}$ that of conventional memories.



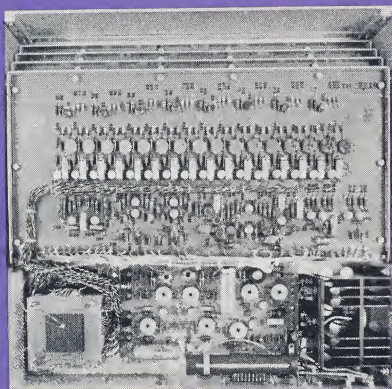
SPECIFIED FOR VALUE

By choosing an optimum number of add and word lengths, a package design has been developed that uses a single, universal circuit board which accommodates the complete range of MINISTORE III capacities. This simplifies manufacturing and reduces the cost of production. Further, MINISTORE III utilizes the voltage levels available in digital systems, thus eliminating the need for separate and costly power supplies.

memory

which cycle is desired. In the load cycle, data must be applied to the data register input.

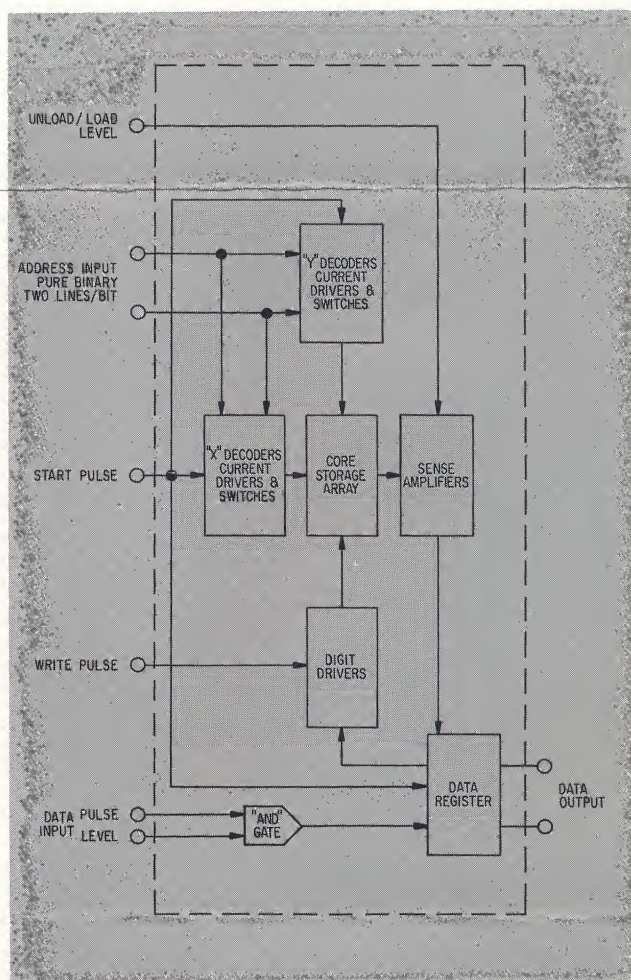
Read/Regenerate Cycle. The Load/Unload level must be at 0 volts. Upon receipt of the start pulse, the data register is cleared and the input address lines interrogate the core stack. The information contained in the addressed cores is read-out and stored in the data register. This information is available within 4 μ secs (access time). At the trailing edge of the start pulse, the write pulse "restores" the information contained in the data register into the cores from which it was taken.



LASTING VALUE

MINISTORE III is inherently more reliable because it uses less active components. Since there are no internal mechanical connectors, the long term reliability is enhanced. Stocking of spare parts is reduced to a minimum. Maintenance is simplified, since there is just one universal board, and each component is clearly designated and easily accessible. A large number of specified check points further facilitates easy maintenance.

Clear/Write Cycle. The Load/Unload level must be at -6 volts. Upon receipt of the start pulse the data register is cleared. The Load level inhibits the sense amplifier gate and prevents the data from being read-out from the addressed cores to the data register.



Data is applied to the data register inputs through a resistor/capacitor gate, affording two options for presenting the data . . . as a pulse or as a level which is clocked in.

During the write portion of the cycle the new data in the data register is written into the memory. The input word must be presented in parallel. The data register holds this word until the start of the next cycle, at which time the start pulse clears the data register.

If desired, the data register reset line can be disconnected from the internal timing and brought out to a pin so that the data register can be reset by external control.

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SPECIFICATIONS

FUNCTIONAL

<i>Capacity</i>	64 to 1024 words
<i>Word Size</i>	2 to 8 bits per word
<i>Access Time</i>	4 μ sec
<i>Full Cycle Time</i>	10 μ sec
<i>Mode of Access</i>	random-parallel
<i>Commands</i>	(1) READ/REGENERATE (UNLOAD) (2) CLEAR/WRITE (LOAD)
<i>Address</i>	straight binary—parallel—two lines per bit
<i>Input Data</i>	MODE: Parallel FORM: Information can be presented as (a) a Level which is clocked in, or (b) in the form of a positive going pulse
<i>Output</i>	MODE: Parallel. Two lines per bit FORM: DC Level

POWER REQUIREMENTS

Negative Voltage:
—15 to —30 volts
4.0 amps maximum
Positive Voltage:
+15 to +30 volts
0.5 amps maximum
These voltages are regulated to ± 12 volts $\pm 1\%$ in the MINISTORE III

MECHANICAL

<i>Size</i>	19" W. x 3½" H. x 16½" D.
<i>Finish</i>	Satin Anodized Aluminum
<i>Connections</i>	All external connections via (2) Amphenol 36 pin micro ribbon connectors
<i>Mounting</i>	Standard relay rack mounted
<i>Cooling</i>	Convection cooled
<i>Weight</i>	20 lbs.

ENVIRONMENTAL

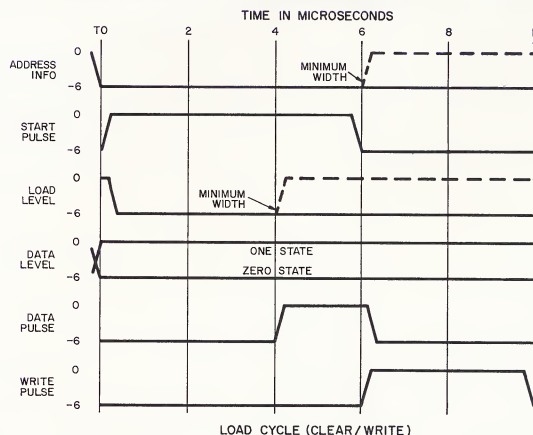
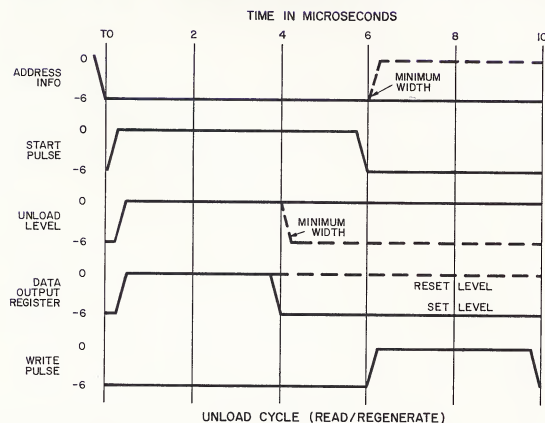
<i>Operating Temp.</i>	0° to +50°C
<i>Storage Temp.</i>	—20° to +60°C
<i>Relative Humidity</i>	0% to 90%

INPUT

<i>Start Pulse</i>	Positive-going pulse (—6 to 0 volts) Pulse width: minimum 6 μ secs Rise and Fall Time: less than 1 μ sec Loading: 15 ma, 1000 pf
<i>Write Pulse</i>	Positive-going pulse (—6 to 0 volts). Must follow the trailing edge of Start pulse to ± 1 μ sec Pulse width: 4 μ secs ± 1 μ sec Rise and Fall Time: less than 1 μ sec Loading: 15 ma, 1000 pf
<i>Load/Unload Level</i>	UNLOAD: 0 volts LOAD: —6 volts A voltage which must be quiescent within .5 μ sec after start pulse and have a minimum width of 4 μ sec Rise and Fall Time: not critical Loading: 15 ma, 1000 pf
<i>Address Information</i>	Pure binary, two lines per bit, must be quiescent during entire period of start pulse TRUE: —6 volts FALSE: 0 volts Rise and Fall Time: not critical Loading: 15 ma maximum, 1000 pf
<i>Data Information</i>	Input through R-C gate 1. Level Input: 0 volts = ONE; —6 volts = ZERO Level must be applied to resistor input at least 2 μ secs before positive-going clock pulse is applied to the capacitor input. The clock pulse width must be greater than 1 μ sec, and Rise and Fall Time less than .5 μ sec Loading: 2 ma, 680 pf 2. Pulse Input: Resistor grounded and positive-going pulse applied to capacitor represents a ONE Data Pulse: between 1 and 4 μ sec duration; .5 μ sec rise and fall time

OUTPUT

Both collectors are available as outputs from the data register
Loading: 10 ma, DC can be delivered from ground; 3 ma, DC can be delivered from —12 volts
Maximum capacitor load: 1000 pf



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engineering, inc. A and Courtland Streets, Philadelphia 20, Pa. / GLadstone 5-9000

May 21, 1964

•Mr. J. Nelson
Consultant
Box 1546
Poughkeepsie, New York 12603

Dear Mr. Nelson:

Thank you for your interest in our Ministore Magnetic Core Memory.

We are pleased to announce that the Ministore III, described in the enclosed catalog sheet, has been expanded in capability. Now available are word sizes to 24 bits in capacities to 256 words, word sizes to 16 bits in capacities to 1024 words and word sizes to 8 bits in capacities to 2048 words.

In all other respects, functionally and physically, the new Ministore IIIA is identical to the Ministore III.

We hope you find this data interesting. If you would like to discuss specific details or would like further information please do not hesitate to contact us.

Very truly yours,

RESE ENGINEERING, INC.

David M. Biberman
President

DMB: jr
Encls.

PRICE LIST

Effective

January 2, 1964

MINISTORE III

10 μ sec. Random Access Memories

		Number of Addresses (words)				
		64	128	256	512	1024
Word Length (Data Bits)	2	\$1000.	\$1300.	\$1500.	\$2200.	\$2600.
	4	1500.	1800.	2000.	2800.	3400.
	6	2000.	2300.	2500.	3400.	4200.
	8	2500.	2800.	3000.	4000.	5000.

Prices in quantities or custom requirements furnished upon request.

Prices subject to change without notice.

Above prices are f.o.b. factory, Philadelphia, Pennsylvania

Ordering information: to purchase a Ministore III memory with a capacity of 512 words and 6 bits per word, specify as follows:

Ministore III - 6 x 512

Unit cost = \$3,400.00